800G QSFP-DD 2xFR4 Transceiver, 2x Duplex LC, 2KM



Features

- Compliant with IEEE 802.3cu-2021:
- 2x400GBASE-FR4 optical interface
- Compliant with IEEE P802.3ck D3.0
- 2x400GAUI-4 C2M electrical interface
- Compliant with QSFP-DD800 MSA HW Rev 6.01 with dual LC connector
- Compliant with CMIS Rev 5.0
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

Application

- 800G 2xFR4
- Data center networks

Ordering Information

Part. No	Specifications							
	Pack	Rate (Gbps)	Receiver	OMA Sensitivity	CMIS	Temp (°C)	Reach (KM)	DDM
ELOM800G-QDD-2F4-S	QSFP-DD	800G	PIN	<-4.6dBm	5.0	0~70	2	Y

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	ºC	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	$\|V_{DIP}-V_{DIN}\|$	-	1	V	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	
Control Output Current	I_O	-20	20	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	ºC	1
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	6800	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	5611	mA	
Maximum Power Dissipation	P_D	-	-	17	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	2	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	2000	m	

Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Transmitter Optical Specifications						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0, L4	λ_{C0}, λ_{C4}	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λ_{C1}, λ_{C5}	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λ_{C2}, λ_{C6}	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Total average launch power	AOP_T	-	-	10.4	dBm	
Average Launch Power, each lane	AOP_L	-3.2	-	4.4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane for TDECQ <1.4 dB for 1.4 dB ≤TDECQ ≤3.4 dB	T_{OMA}	-0.2 –1.6 + TDECQ	-	3.7	dBm	
Difference in launch power between any two lanes (OMAouter)	AOP_d	-	-	3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	3.4	dB	
| TDECQ – TECQ |	-	-	-	2.5	dB	
Over/under-shoot	-	-	-	22	%	
Transmitter power excursion	-	-	-	1.8	dBm	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-16	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter transition time (max)	Tr	-	-	17	ps	
$RIN_{17.1}$OMA (max)	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	17.1	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	2

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Transmitter reflectance is defined looking into the transmitter

Receiver Optical Specifications						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0, L4	λ_{C0}, λ_{C4}	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λ_{C1}, λ_{C5}	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λ_{C2}, λ_{C6}	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Damage Threshold, each Lane	AOP_D	5.4	-	-	dBm	
Average Receive Power, each Lane	AOP_R	-7.2	-	4.4	dBm	
Receive Power (OMAouter), each Lane	OMA_R	-	-	3.7	dBm	
Difference in receive power between any two lanes (OMAouter) (max)	AOP_g	-	-	4.1	dB	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver sensitivity (OMAouter), each lane for TECQ < 1.4 dB for 1.4 dB≤TECQ ≤3.4 dB	S_{OMA}	-	-	-4.6 –6 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-2.6	dBm	1
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	
OMAouter of each aggressor lane	-	-	1.4	-	dBm	

Note 1: Measured with conformance test signal at TP3 for the BER = 2.4x10-4

Functional Characteristics (Electrical)

Electrical Specification High Speed Signal (compliant with IEEE802.3ck C2M)

Receiver (Module Output, TP4)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
AC common-mode output Voltage (RMS)	-	-	-	25	mV	
Differential peak-to-peak output voltage Short mode Long mode	-	-	-	600 845	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Transmitter (Module Input, TP1)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
AC common-mode RMS voltage tolerance (TP1a)	-	25	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

Electrical Specification Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Max.	Unit	Condition
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

Pin Definitions

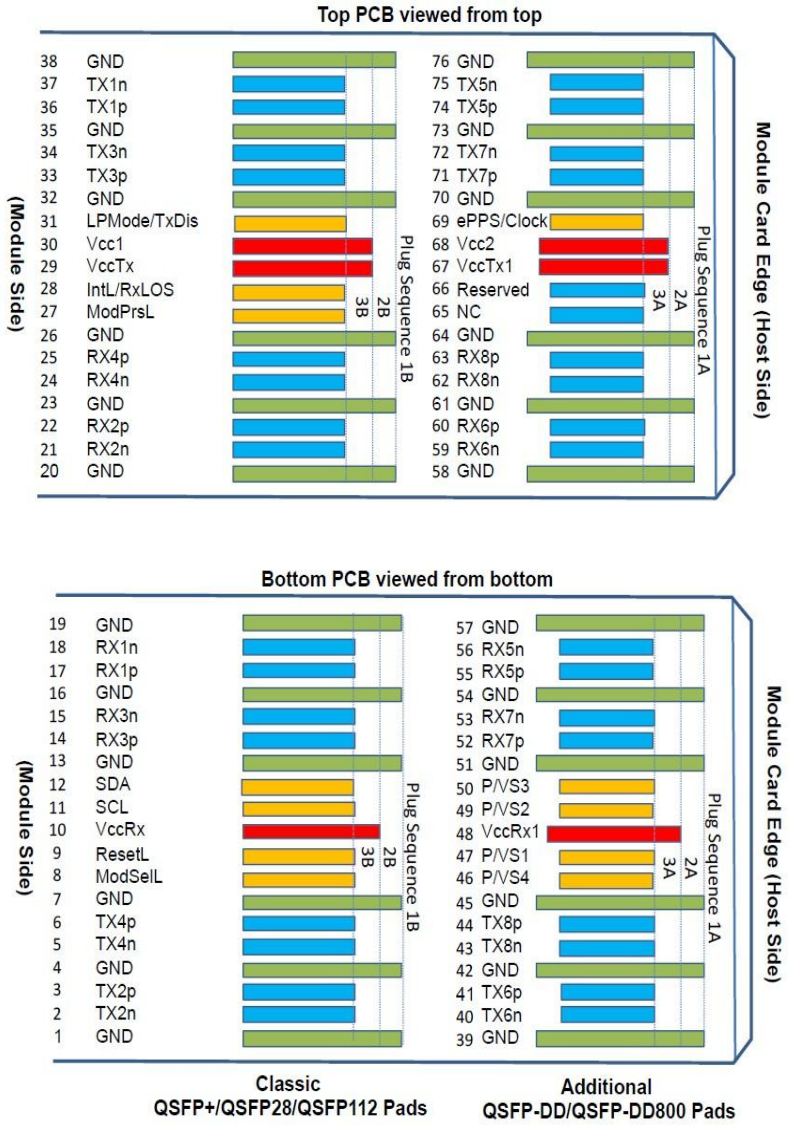


Figure 1 – Pin definitions of the module high speed inputs/output

Module Pin Definitions

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	TWI serial interface clock	49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS-I/O	SDA	TWI serial interface data	50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output

26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

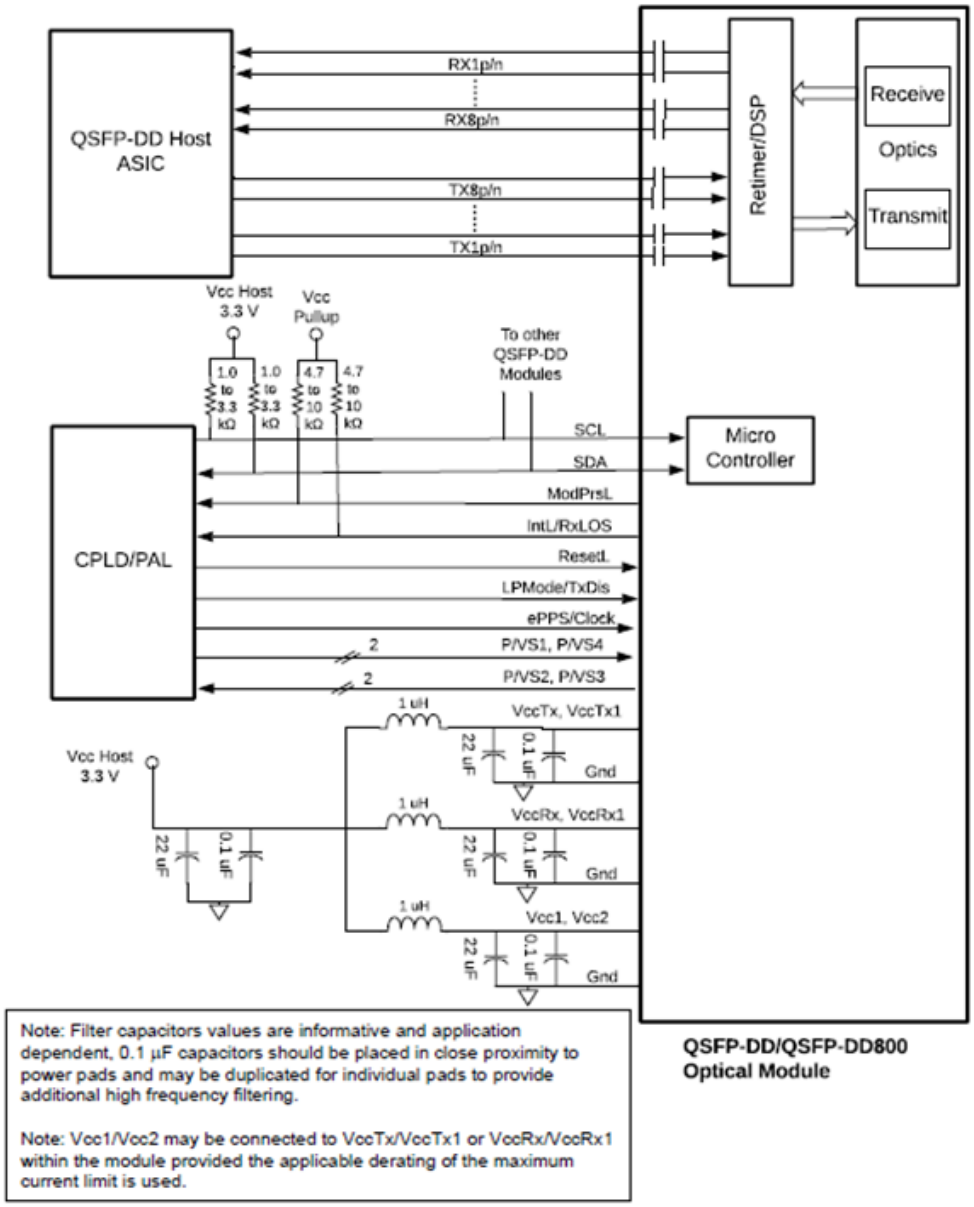
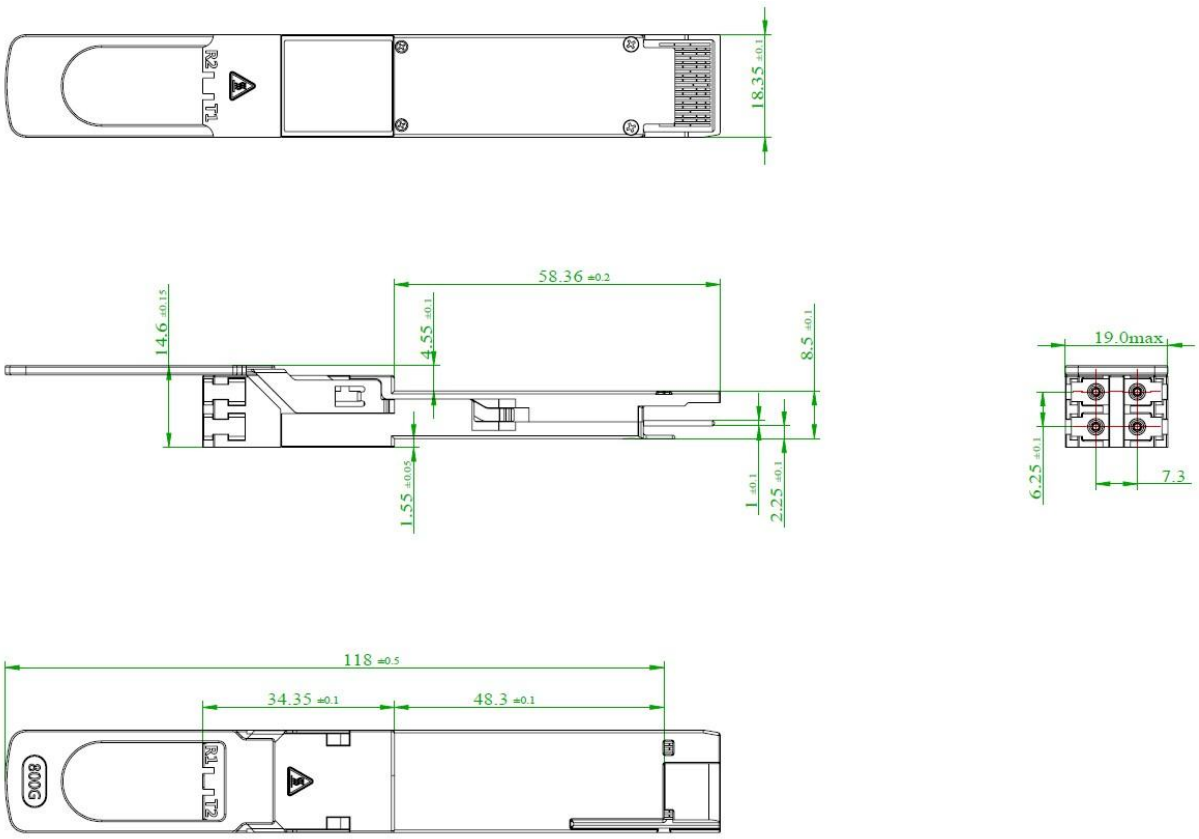


Figure 2 – Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	℃	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-3.2 to +4.4	±3	dB	Internal
Rx Receive Power (Each Lane)	-7.2 to +4.4	±3	dB	Internal

Mechanical Diagram



Regulatory Compliance

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1:2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1:2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014